Field Programmable Gate Array Based Phase Shift Technique For Three Phase Inverter

S. K. Rathod[1], M.D. Uplane[2], P.K. Gaikwad[3]

[1]Department of Electronics, Smt. Kasturbai Walchand College, Sangli, Maharashtra, India

[2]Department of Instrumentation Science, Savitribai Phule Pune University, Pune, Maharashtra, India

[3]Department of Electronics, VLSI Laboratory, Shivaji University, Kolhapur, Maharashtra 416 004, India

Abstract

The research paper deals with design and development of Soft Intellectual Property (IP) Core to generate electrical signals for interfacing unit of three phase inverter. The Field Programmable Gate Array (FPGA) was hardwired with the Soft IP Core. It produces the necessary square-wave signals to drive the interfacing module between MOSFET based three phase inverter and low power digital circuit. A square-wave cycle of 360 degree was divided in three phases of 120 degree. During each phase, an appropriate bus-signal was generated from FPGA core, so that the interfacing circuit would fire a pair of MOSFETs connected in three phase inverter. For that, the source code was developed in Very High Speed Integrated Circuit Hardware Description Language (VHDL). The finite state machines (FSM) were coded in two processes of VHDL architecture to produce necessary timing signals for three phase inverter driver.

Keywords: *Three-phase inverter, FPGA, VHDL, MOSFET, phase shift.*

1. Introduction

The basic three-phase inverter bridge can be controlled with each switch conducting for 120°. As a result, at any instant only two switches conduct. A 60° (⅓π), dead time exists between two series switches conducting, thereby providing a safety margin against simultaneous conduction of the two series devices across the dc supply rail [1]. The step of process of generating Pulse Width Modulation (PWM) has been reported in [2] and was implemented by using a microcontroller 89c51 and using personal computer (PC). In that the unipolar modulation technique is presented. The generated pulses fed to a bridge inverter consist of six Metal Oxide Semiconductor Field Effect Transistor (MOSFET) devices. The research work reported in [3] uses PIC microcontroller based PWM inverter controlled four switch three phase inverter (FSTPI) fed Induction Motor drive. Simulation and experimental work are carried out and results presented to demonstrate the feasibility of the proposed approach. Simulation is carried out using MATLAB SIMULINK and in the experimental work a prototype model is built to verify the simulation results. Another researcher reported [4] a microcontroller based advanced technique of generating sine wave with lowest harmonics is designed and implemented. The main objective of the proposed technique was to design a low cost, low harmonics voltage source inverter. The project uses PIC16F73 microcontroller to generate 4 KHz PWM switching signal. The design is essentially focused upon low power electronic appliances such as light, fan, chargers, television etc.

Taking various ideas of three phase inverter mentioned in above paragraph, the present paper deals with design and FPGA implementation of soft Intellectual Property (IP) core produce three signal-lines; each of it having a phase difference of 120° to drives a pair of MOSFETs and deliver the power to the load. Most of the electrical devices in India are operated on 50Hz. Therefore, the square-wave frequency of the order of around 50 Hz was fed to the inverter driving circuit. The complete cycle of 20 ms was divided equally in three time-spans of 6.7ms. Each of the signals produces the 'on-time' of 4ms, and the 'off-time' of the interval of 2.7ms. In other words, each pair of the MOSFETs (connected in inverter circuit) was turned on for 4ms, and it was commutated 2.7ms earlier to firing next pair of the power devices.

The main reason behind selecting FPGA platform to drive a MOSFETs based three-phase inverter is that, this hardware technology is enough capable to execute all the processes in a concurrent manner, instead of using routine practices of microcontroller based systems; which are sequential in nature. The Xilinx FPGA Virtex-5 was the target device for implementation of the soft IP core. The design flow was accomplished by EDA tool Xilinx ISE 14.6. The process of simulation was carried out using the integrated tool 'ISim'. Following to the design process, the

core was synthesized, implemented and finally the tool generated bit-file was downloaded in the said device memory, using 'Adept' tool from the Digilent technology.

2. VHDL FSM and Soft IP Core Development

The finite state machine (FSM) shown in Fig.1 illustrates six states, namely s0 through s5. The state transition takes place only when a desired condition for specific delay is satisfied; otherwise it remains in its current state and produces predefined the three-bit signal. The FSM waits for either 4ms or 2.7ms in its specific state; before taking progresses towards the next state. It was necessary that, each pair of the MOSFETs connected in three phase inverter circuit stay fired (i.e. ON) for 4ms, and therefore, only one output (out of thee bit vector) from FPGA may be asserted high. On the other hand, the FPGA provides low signals at its all inverter-driving lines and wait for 2.7ms; before the next pair of MOSFETs would turn on. The firing of subsequent MOSFETs pair takes place at every 120°.

The VHDL source code deployed here contains a clock divider module as given in [5]. It is a divide by 1000 counter-module that accepts the clock source of 100 MHz available on the Virtex-5 FPGA board and produces the 100 KHz output signal. This clock divider module was instantiated in the top level entity and the clock of 100 KHz was used for generating necessary delays of 4ms and 2.7ms.
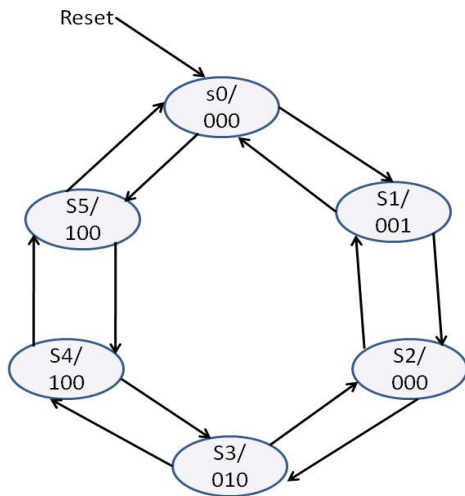

Fig. 1 Finite State Machine to design FPGA based three phase inverter driver Proposed beam former.

It was tested on oscilloscope that, the 100 KHz clock signal generated from FPGA output line shows the frequency signal of 10 µs. To provide the delay of 2.7ms, it may count 270 (10D in hexadecimal) clock pulses of 10 µs. Similarly to produce a delay of 4ms, the 10 µs clock travels through 400 (190 in hexadecimal) pulses.

During an initial delay of 2.7ms, the FPGA core produces "000" output which was fed to the input of three phase inverter driver, so that none of the MOSFETs would be fired. This state in FSM (as shown in Fig.1) is referred to as 's0' and the signal in VHDL lines of source code given below is named as 'T0'. In the architecture declaration part of VHDL code, there are six internal signals (T0 through T5) initialized with necessary values applicable to generate delays in each states, 's0' to 's5':

$$T0 <= X"10D"; \text{ -- for s0,}$$
$$T1 <= X"29D"; \text{ -- for s1,}$$
$$T2 <= X"3AA"; \text{ -- for s2,}$$
$$T3 <= X"53A"; \text{ -- for s3,}$$
$$T4 <= X"647"; \text{ -- for s4,}$$
$$T5 <= X"7D7"; \text{ -- for s5.}$$

For example, to generate a delay of 6.7ms (i.e. 2.7ms+4ms) the count value stored in signal 'T1' becomes 29D in hexadecimal. The state variable in this case is 's1'. During this state the FSM produces "001" output at the FPGA output pins to fire only one pair of the MOSFETs.

The VHDL based FSM has two processes working in parallel with a common clock of 100 KH. The process named as 'N_State' travels from its current-state to the next-state after the particular condition of delay is fulfilled. Another process produces only three-bit output; which is necessary to drive one pair of MOSFETs at a time.

3. Simulation Results

The simulation process was accomplished using Xilinx Simulation tool: ISim which is provided in the Xilinx ISE EDA tool itself. The top level module of the system consists of reset input, global clock and a 3-bit output for driving three phase inverter system. The Fig.2 illustrates the simulation results with different states through which the FSM travels. It also shows that, three phase driver lines are asserted high one at a time, whereas other two lines are idle to low

The Fig.2 shows a simulation result obtained using Xilinx ISE simulator: ISim. The simulation window depicts various inputs and output as well as some internal signals of VHDL architecture; designed for three phase inverter driver. The reset input 'rst', global clock signal 'clk' and three phase driver signal named as 'phase[2:0]' are shown

on the left pane of simulation window. The prime goal of designing such soft IP core was to generate a three-bit vector signal.
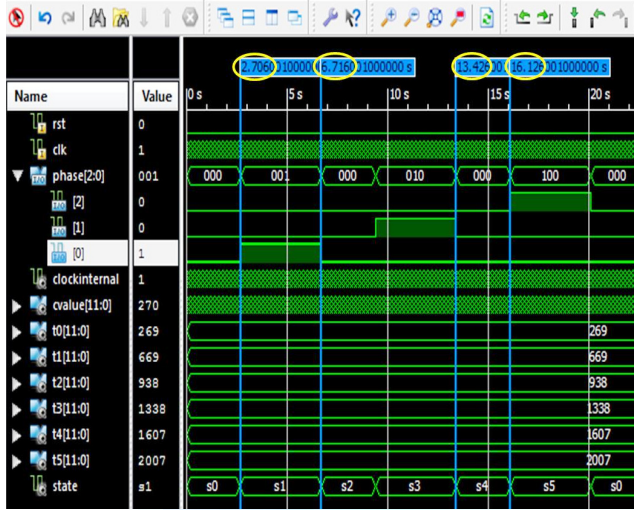

Fig. 2 Simulation results for three phase inverter driver observed using Xilinx ISE Isim Simulator.

The Fig.2 illustrates two pairs of vertical markers to note the time difference; related to 4ms and 2.7ms. The ON time of each three phase inverter driver line is 4ms. In present case the 'phase[0]' signal is marked at two time-axes; first for 2.706 and next for 6.710. Thus a time difference results to 4.01ms; during the state 's1' of the FSM. Similarly, another pair of time scale pointers (during state 's4') indicates the time difference of 2.7ms; which reveals that, the state machine stays for said time-delay; before the next phase signal is asserted HIGH to turns on another pair of MOSFETs in the inverter circuit. Other internal signals like 't0' through 't5' are also seen in the screen-shot of simulation window, but these signals are initialized with individual values used to generate different time delays according to states 's0' through 's5'.
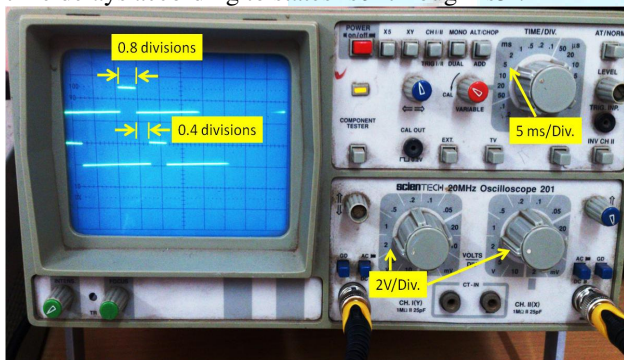

Fig. 3 Waveforms on oscilloscope showing different phase shift signals to drive three phase inverter.

4. Hardware Testing of the Complete Setup

For final testing of the FPGA based three phase inverter driver, the printer circuit board (PCB) was developed according to the circuit described in [6]. And the base drive unit was also assembled with the help of circuit diagram reported in [7]. The Fig.3 shows two waveforms tested for three phase inverter. There are three such signals generated from FPGA output lines; however limitations of a dual channel oscilloscope confines it to visualize maximum two waveforms, therefore only two signals are seen on the display unit. To drive a MOSFET based three phase inverter, it is necessary to provide a three-bit signal at the input of its interfacing unit; as shown in Fig.4. Each consecutive signal has a phase shift of 120 degree. And Fig.3 illustrates two signals having the same phase shift between them. To drive the electrical appliances that work on 50 Hz, the complete cycle of 20 ms was divided into three time-spans of 4ms and 2.7ms. The Fig.3 shows both waveforms have 0.8 divisions on time scale, and the TIME/DIV knob of the oscilloscope was set to 5ms. This results to 4ms delay for 'High' time. The moment when first signal goes high to low, there is similar transition of another signal; but after the time interval of 2.7ms, as shown in Fig.3.

The Fig.4 shows the Xilinx FPGA Virtex-5 board manufactured by Digilent Inc [8]. There is a three bit signal given to the interfacing module; playing the role of isolation between high-power MOSFETs inverter and low-power operated FPGA device; hosted on the 'Genesys' board. This interfacing unit comprises of the Darlington pair by integrated circuit, IC: MCT2E device at the input side. The collector output of this chip is fed to a MOSFET driver IC IR2110 [9]. The three-phase inverter is also shown connected to the MOSFET driver. From the view point of prototype development a DC motor was connected as a load for the inverter.
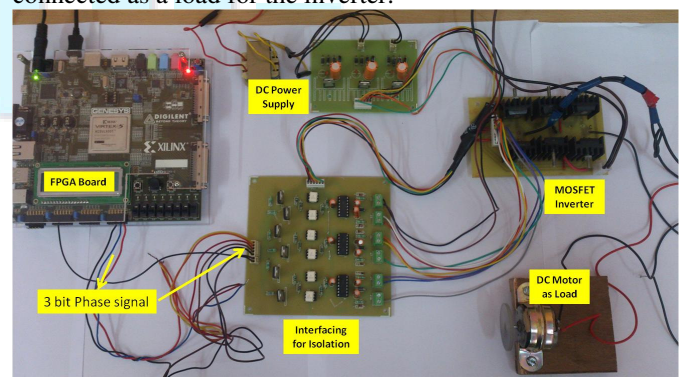

Fig. 4 FPGA based Three Phase inverter system with dc motor as a Load.

5. Conclusions

The prime objective behind this research work is to portray the idea of implementing an FPGA based development and implementation of soft IP core to generate three different signals with an equal phase shift of 120 degree. Such signal engendering from a reconfigurable device like Xilinx FPGA drive a three-phase MOSFET based inverters efficiently. The HDL based source code comprises of a clock divider module; instantiated in the top level entity consisting of VHDL architecture body with two concurrently executing processes. One process was to test the necessary time delays for taking state transition and the latter was to produce three-bit signal driving the inverter interfacing unit. There is future scope for this work by generating Pulse Width Modulations during the ON times of each phase signal and control the speed of the DC motor which was connected as a load in this research work..

References

[1] https://www.google.co.in/url?sa=t&rct=j&q=&esrc=s&source=web&cd=4&cad=rja&uact=8&ved=0CDAQFjADahUKEwj4qMjDsK3HAhWHC44KHWhGCFI&url=http%3A%2F%2Fhomepages.eee.strath.ac.uk%2F~bwwilliams%2FBook%2FChapter%252014.pdf&ei=52PQVbiZOoeXuATojKGQBQ&usg=AFQjCNFIhgLEn0yRIv1gzOvd6fdu2AgwDg.

[2] Mohammed Hussein Baqir, "Generation of PWM Inverter Based on a Microcontroller at Feeding Induction Motor", International Journal of Soft Computing and Engineering (IJSCE), ISSN: 2231-2307, Volume-4, Issue-1, pp.9-14, March 2014.

[3] Mohanty Kant Nalin, Muthu Ranganath, "Microcontroller based PWM controlled four switch three phase inverter fed induction motor drive", Serbian Journal of Electrical Engineering 2010 Volume 7, Issue 2, pp. 195-204A. Name, "Dissertation Title", M.S.(or Ph.D.) thesis, Department, University, City, Country, Year.

[4] A. A. Mamun, M. F. Elahi, M. Quamruzzaman, M. U. Tomal, "Design and Implementation of Single Phase Inverter", International Journal of Science and Research (IJSR), India Online ISSN: 2319-7064, Volume 2 Issue 2, pp.163-167, February 2013.

[5] Support Document, "Xilinx ISE demo project for the PmodAD2 and a PmodDA1", Digilent, Inc., Pullman, WA 99163-0428, November 2011, DSD-0000321, viewed 23 August 2015 from https://www.digilentinc.com/Products/Detail.cfm?NavPath=2,1040,1046&Prod=PMOD-AD2

[6] Viewed 10 august 2013 from https://www.google.co.in/search?q=three+phase+inverter+using+mosfet&espv=2&biw=1600&bih=799&tbm=isch&imgil=9WWeTuTdyNlGLM%253A%253Bf0NXVacXXdvT2M%253Bhttp%25253A%25252F%25252Fwww.embedded.com%25252Fprint%25252F4012241&source=iu&pf=m&fir=9WWeTuTdyNlGLM%253A%252Cf0NXVacXXdvT2M%252C_&usg=__2R28crtUkf7NHn7Dr7-P6NWszrA%3D&ved=0CCgQyjdqFQoTCLuWlKWxxscCFQ4GjgodQXEFlA&ei=JoDdVbvrBI6MuATB4pWgCQ#imgrc=9WWeTuTdyNlGLM%3A&usg=__2R28crtUkf7NHn7Dr7-P6NWszrA%3D

[7] S.K. Rathod, "Design and Development of Remote Controlled Switching System for Single Phase Induction Motor Drive Using PLC", A Project report submitted to UGC Minor Research Project, 2011-13, pp. 50-51

[8] Support Document, "Genesys Virtex-5 FPGA Development Board", Part number: 410-138P-KIT, viewed August 21, 2013, from https://www.digilentinc.com/Products/Detail.cfm?NavPath=2,400,819&Prod=GENESYS

[9] Data sheet viewed August 23, 2014 from http://www.daedalus.ei.tum.de/attachments/article/257/IR2110_IR2110S_IR2113_IR2113S.pdf